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ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 07/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/091,776	KIMURA, KATSUJI	
	Examiner	Art Unit	
	Terry L Englund	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *May 14, 2004, and Jul Interviews*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-14,17-25 and 27-31* is/are pending in the application.

4a) Of the above claim(s) *12-14 and 22-25* is/are withdrawn from consideration.

5)☒ Claim(s) *2-11,17-21 and 27* is/are allowed.

6)☒ Claim(s) *28-31* is/are rejected.

7)☒ Claim(s) *18 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 May 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *07232004*.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

The amendment submitted May 14, 2004 was reviewed and considered with the following results:

The amended claims overcame all of the objections to claims 3, 4, 7-11, and 18-20 described in the previous Office Action. Therefore, those objections have been withdrawn. However, when reconsidering the amended claims, two other objections were noted with respect to claims 18-19. Those objections are described later under the appropriate section.

Amended claim 31 overcame its rejection under 35 U.S.C. 112, second paragraph, which has now been withdrawn.

The prior art rejections of claims 28-31 were not overcome by the applicant's arguments and comments. Therefore, those rejections have been maintained, and are described later under the appropriate section. Related comments are described under the Response to Arguments/ Comments section.

Claim Objections

Claims 18-19 are objected to because of the following informalities: Claim 18, line 25 "the other of the" should be --the other-- to improve word flow, and also to minimize confusion with respect to the phrase might be implying there may be more than one "other MOS transistor" within a differential pair. The drain connection recited on line 37 of claim 19 can be confused with the drain related connection cited in the previous line. Therefore, it is suggested "pair with said drain" on lines 36 be changed to --pair, with said drain of the other MOS transistor of the (K2 + 1) differential pair--. [For example, using the applicant's own Fig. 6 as a reference, the

(K2 + 1) pair corresponds to M(2K2_1),M(2K2+2), wherein the drain and gate of one MOS transistor M(2K2+1) is connected to the drain of MOS transistor M(2K2) in the K2 differential pair M(2K2-1),M2K2), and it is the drain of the other MOS transistor M(2K2+2) within the (K2+1) differential pair that is actually connected to output end MN03 of current mirror MN02,MN03 to provide reference voltage VREF.] Appropriate corrections are required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 28-29 remain rejected under 35 U.S.C. 102(b) as being anticipated by McNeill et al. (McNeill), a reference cited in the previous Office Action. Fig. 1 shows a CMOS reference voltage circuit for generating and outputting reference voltage VBG. The circuit comprises first/second diode-connected transistors Q1/Q2 respectively grounded and driven by two constant currents 10μA and 80μA with a constant current ratio (e.g. 1:8); and means 112,114, 170,116,124 for amplifying (e.g. by 112) a differential voltage between output voltages (on nodes N1,N2) of diode-connected transistors Q1,Q2, and summing (e.g. by 116) a resulting amplified voltage with output voltage (on node N2) of diode-connected transistor Q2. The means comprises what can be deemed first/second operational transconductance amplifiers with respect to circuitry found within amplifiers 112,116 (as explained later), and a current mirror circuit (e.g. M3,170) connected between the first/second OTAs. Although McNeill does not clearly disclose an OTA, one of ordinary skill in the art would understand that what could be

considered an OTA does exist within each of amplifiers 112 and 116. For example, column 7, lines 34-35 clearly indicate Figs. 4A and 4B "may be used for VAMP1 112 and VAMP2 116." Using Fig. 4A as an example, the OTA can be considered most of the components shown within the figure. The OTA is biased by a current provided by a transistor (not labeled), which in turn is biased by voltage VBIAS, and the other unlabeled transistor biased by voltage VBIAS is used as a resistive element to convert the current output by the OTA's lower right transistor (also unlabeled) to a voltage output provided at OUT. Therefore, one of ordinary skill in the art would understand that the first OTA (of amplifier 112) receives the differential voltage from the diode-connected transistors, amplifies the difference, and effectively provides a related current to current mirror 170, wherein the second OTA (of amplifier 116) has first input terminal + receiving the output voltage from diode-connected transistor Q2, and second input terminal – is connected to the output terminal (via 124) of the second OTA and is driven by a current (via 170) proportional to an output current of the first OTA, wherein an output terminal voltage VBG of the second OTA is the reference voltage. This anticipates claim 28. Since diode-connected transistors Q1 and Q2 are both bipolar transistors, claim 29 is also anticipated.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 30 and 31 remain rejected under 35 U.S.C. 103(a) as being unpatentable over McNeill et al. (McNeill). Fig. 1 of McNeill shows a reference voltage circuit comprising

first/second diode-connected PNP bipolar transistors Q1/Q2 each having a base connected to a collector, and each being fed with a respective constant current (i.e. 10μA/80μA); first/second operational transconductance amplifiers within amplifiers 112/116 (as previously described), each having first/second input terminals (e.g. +/-), and adapted to effectively output from an output terminal a current proportional to a differential voltage applied to the first/second input terminals; and a current mirror circuit 170 having at least an input end 120 and an output end 122, with a ratio of the input current to output current being a predetermined value (e.g. 1:1). Although the reference shows the bipolar transistors Q1/Q2 as PNP transistors, McNeill does disclose that the invention is not limited to their use (e.g. see column 3, lines 51-53). Therefore, it would have been obvious to one of ordinary skill in the art to replace each of diode-connected PNP transistors Q1/Q2 with a corresponding diode-connected NPN transistor. With these diode-connected transistors, one of ordinary skill in the art would know they would comprise emitter-grounded bipolar transistors (to ensure they would be forward biased), wherein the base/collector of Q1 would be coupled to N1 via 110 to receive constant current 10μA, and the base/collector of Q2 would be connected to N2 to receive constant current 80μA. With such a configuration, the collectors of first/second NPN bipolar transistors Q1/Q2 would be connected to respective first/second input terminals of the first OTA within amplifier 112 as previously described, with the output terminal of the first OTA connected to input end 120 via M3. Output terminal N4 of second OTA within amplifier 116, and the collector of diode-connected NPN bipolar transistor Q2, are respectively connected to first (-) and second (+) input terminals of the second OTA. Since the first input terminal (-) and output terminal N4 of second OTA (116) are connected to output end 122 of current mirror circuit 170, and output terminal N4 outputs reference voltage

VBG, claim 30 is rendered obvious. The replacement of diode-connected PNP transistors Q1/Q2 with diode-connected NPN transistors replaces one type of diode with another type of diode, wherein each type provides a diode junction and a related diode voltage drop. Since each diode-connected NPN transistor is both an emitter-grounded bipolar transistor, and a cathode-grounded diode (to ensure a forward diode voltage drop), the limitations recited within claim 31 are also rendered obvious. [Note: Details are not provided here since the limitations basically take the first/second emitter-grounded bipolar transistors of claim 30, and re-identifies them as an emitter-grounded bipolar transistor and cathode-grounded diode, respectively.]

Allowable Subject Matter

Other than each of claims 18-19 containing the objection described above, claims 2-11, 17-21, and 27 are allowable. There is presently no strong motivation to modify or combine any prior art reference(s) to ensure the reference voltage circuit comprises: 1) the first/second OTAs with equal transconductances, and the current mirror circuit has a current ratio of 1:K2 with K2>1 as recited within independent claim 2; 2) the first/second OTAs have transconductances set so gm1 = K2xgm2 with K2>1, and the current mirror circuit's current ratio is 1:1 as recited within independent claim 3; 3) the first/second OTAs have transconductances set at gm1 = K3xgm2 with K3>1, and a current ratio of the current mirror circuit set to 1:K2 with K2>1 as recited within independent claim 4; 4) the means for amplifying/summing comprises (K2+1) differential pairs as recited within independent claims 5-6; 5) one of the transistors within the second differential pair is diode-connected and driven by a current proportional to an output current of one transistor of the first differential pair as recited within independent claim 7; (upon which claims 8-11 depend); 6) the reference voltage output is given by VBE2 + {K2 x ΔVBE x

gm1}/gm2 as recited within independent claim 17; 7) the current mirror circuit has a plural number of output ends, and the reference voltage circuit also comprises third to (K2+1) differential pairs as recited within independent claim 18 (upon which claim 20 depends); 8) first/second current mirror circuits, as well as first to (K2+1) differential pairs of MOS transistors, wherein K2≥3, as recited within independent claim 19 (upon which claim 27 depends); and 9) the second differential pair of MOS transistors has one transistor with its gate and drain connected together with the output end of the current mirror circuit as recited within independent claim 21.

Claims 12-14, and 22-25 had been previously withdrawn for consideration.

Claims 1, 15, 16, and 26 have been cancelled.

Response to Arguments/Comments

Applicant's arguments filed May 14, 2004 have been fully considered but they are not persuasive. The arguments are: 1) "McNeill et al. discloses an operational amplifier, but never discloses an operational transconductance amplifier" and "an OTA receives a differential input voltage and outputs a current"; and 2) the present invention does not require resistors

1) The basic premise with respect to the first set of arguments relate to what can be considered a transconductance amplifier. This examiner believes each amplifier has its own inherent transconductance, whether a reference clearly discloses it or not. Therefore, each amplifier can be considered one type of a transconductance type amplifier. With respect to the McNeill reference, the examiner agrees that the reference of McNeill does not cite an OTA, or operational transconductance amplifier, by a label. However, the applicant's comments with respect to an OTA being biased by an input current, and receiving a voltage input and providing

an output current will now be explained again with respect to how the examiner interprets the operation of McNeill's amplifiers. Each of Fig. 1's amplifiers 112 and 116 can be the amplifier shown in Fig. 4A (e.g. see column 7, lines 34-36). One way to consider each of these amplifiers is by considering it to have an OTA, a biasing current source, and a resistive element for converting a current to a voltage. For example, the OTA can be considered as comprising all of the elements shown except for the two transistors biased by voltage VBIAS. Therefore, the OTA comprises a pair of MOS input transistors (shown receiving the differential input signals VIP/VIN) having common sources receiving a bias current from the current source formed by the upper left transistor receiving VBIAS. The pair of MOS input transistors amplifies, and using a current mirror, provides an output current via the lower right transistor. That output current is converted into a voltage by the upper right transistor biased by VBIAS. Therefore, each amplifier 112/116 of McNeill can be considered as comprising one type of operational transconductance amplifier biased by a current, wherein the OTA converts a differential input voltage into an output current. Also, the first amplifier could be interpreted as comprising 112,114, wherein input differential voltages (corresponding to N1 and N2) are converted into a current (e.g. 20μA) which is applied to the input of current mirror 170.

Another way to consider how McNeill's amplifiers differ from the transconductance amplifier of the applicant is to consider the applicant's own amplifier 12 shown in Fig. 1. Its output is clearly shown as providing reference voltage VREF. Therefore, where is the output current? If voltage VREF is considered as being a result of the amplifier's output current flowing through some type of resistance connected to the output, then the reference voltage will vary of the output resistance is varied. With respect to an OTA receiving a differential input

voltage, and providing an output current, page 24 then states "This difference can be seen more clearly by comparing FIG. 1 of McNeill et al. to FIG. 1 of the instant invention." Comparing the applicant's amplifier 12 with McNeill's amplifier 116, if the applicant believes their own (transconductance) amplifier 12 provides an output current with respect to reference voltage VREF, why can't the examiner believe McNeill's amplifier 116 also provides an output current with respect to reference voltage VBG, and thus consider amplifier 116 as one type of transconductance amplifier? As clearly shown in both figures, and understood by one of ordinary skill in the art, the applicant's amplifier 12 and McNeill's amplifier 116 both receive a differential input voltage.

Therefore, it appears the OTA (or operational transconductance amplifier) label is the most distinguishing feature that the applicant apparently believes prevents McNeill's circuit from reading on some of the rejected claims. However, as described above, that argument is not persuasive.

2) In response to the applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., no resistors are necessary in the present invention) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Also, since the claim's preamble recites "including" (claim 28) or "comprising" (claim 30), this does not prevent a reference from having a resistor. In the case of McNeill's reference, resistor 124 (R2) is coupled between the output of amplifier 116 and its inverting input. Therefore, even with the resistor in place, the amplifier still has its output coupled to its input terminal.

For the reasons described above, the rejections described in this action, and in previous actions, are deemed proper.

THIS ACTION IS MADE FINAL. The applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication, or previous communications, from the examiner should be directed to Terry L. Englund whose telephone number is (571) 272-1743. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (571) 272-1740.

The new central official fax number is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-1562.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TLE

Terry L. Englund

24 July 2004

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